PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte Furukawa

Appeal No. _____

Appellant:	Furukawa et al.
Serial No.:	10/767,065
Filed:	January 29, 2004
Art Unit:	2811
Examiner:	Ori Nadav
Title:	**VERTICAL NANOTUBE SEMICONDUCTOR DEVICE STRUCTURES AND METHODS OF FORMING THE SAME**
Confirmation No.:	5663
Attorney Docket:	ROC920030268US1

Cincinnati, OH 45202 October 27, 2006

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

I hereby certify that this correspondence for Application No. 10/767,065 is being electronically transmitted to Technology Center 2811, via EFS-WEB, on October 27, 2006.

/William R. Allen/
William R. Allen, Reg. No. 48,389

October 27, 2006
Date

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BRIEF ON APPEAL

I. Real Party in Interest

The real party in interest is International Business Machines Corporation of Armonk, New York, which is the assignee of the present invention.

II. Related Appeals and Interferences

There are no related appeals or interferences known to Appellants or Appellants' legal representative that will directly effect or be directly effected by or have a bearing on the decision of the Board in the present appeal.

III. Status of the Claims

Claims 1-6, 8-10, and 25-28 are rejected and claims 7, 11-24, and 29-33 are cancelled. Claims 1-6, 8-10, and 25-28 are now on appeal.

IV. Status of Amendments

There have been no amendments filed subsequent to the final rejection dated August 3, 2006.

V. Summary of Claimed Subject Matter

Appellants' independent claim 1 is directed to a semiconductor device structure (42). *See* Figures 1-8; page 5, lines 4 to page 11, lines 7. As best shown in Figure 8, the device structure (42) comprises a substrate (12) defining a substantially horizontal plane, a source region (10), a drain region (40), and a gate electrode (30) disposed on the substrate (12). The gate electrode (20) is electrically insulated from the substrate (12). The gate electrode (30) is positioned vertically between the source region (10) and the drain region (40). The semiconductor device structure (42) further comprises at least one semiconducting nanotube (14) including a first end (18) electrically coupled with the source region (10), a second end (16) electrically coupled with the drain region (40), and a channel region extending vertically through the gate electrode (30) between the source region (10) and the drain region (40). The channel region is electrically insulated from the gate electrode (30) by gate dielectric (22). The gate electrode (30) is configured to receive a control voltage effective to regulate current flow through the channel region of the at least one semiconducting nanotube (14) between the source region (10) and the drain region (40).

Appellants' independent claim 25 is directed to a semiconductor device structure (50). *See* Figures 1, 2, 9, 10; page 11, lines 8-25. As best shown in Figure 10, the semiconductor device structure (50) comprises an electrically-conductive first plate (10) on the substrate (12), an electrically-conductive second plate (52) disposed vertically above the first plate (10), and an electrically-conductive layer (24) disposed between the first and second plates (10, 52). The semiconductor device structure (50) further comprises at least one nanotube (14) having an end (18) electrically coupled with the first plate (10) for increasing an effective area of the first plate (10). The at least one nanotube (14) is positioned in the electrically-conductive layer (24). The

semiconductor device structure (50) further comprises a dielectric layer (22) coating the length of the at least one nanotube (14) such that the at least one nanotube (14) is electrically isolated from the electrically-conductive layer (24) and the second plate (52).

VI. Grounds of Rejection to be Reviewed on Appeal

1. Claims 25-28 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Pat. No. 6,250,984 to Jin et al. (hereinafter *Jin*).

2. Claims 1, 4-6, 8, and 10 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,858,891 to Farnworth et al. (hereinafter *Farnworth*).

3. Claims 2, 3, and 9 stand rejected under 35 U.S.C. § 103(a) as unpatentable over *Farnworth.*

VII. Argument

Appellants respectfully submit that the Examiner's rejections of claims 1-6, 8-10, and 25-28 are not supported on the record, and that the rejections should be reversed.

A. *Claims 25-28 were improperly rejected under 35 U.S.C. § 102(b) as being anticipated by Jin.*

The Examiner argues that *Jin* anticipates claims 25-28. Anticipation of a claim under 35 U.S.C. § 102, however, requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros., Inc. v. Union Oil Co., 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), *quoted in* In re Robertson, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999). Absent express description, anticipation under inherency requires extrinsic evidence that makes it clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991), *quoted in* In re Robertson at 1951. "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Continental Can at 1749, *quoted in* In re Robertson at 1951.

Appellants respectfully submit that *Jin* fails to anticipate claims 25-28 and, as such, the rejections thereof should be reversed. Appellants will hereinafter address the various claims that are the subject of the Examiner's rejection in order.

Independent Claim 25

On pages 2 and 3 of the August 3, 2006 Office Action, the Examiner refers to Figure 11 of *Jin* and reproduces Appellants' independent claim 25 to contend that *Jin* discloses (indented for clarity):

> a substrate (105);
> an electrically conductive first plate (104) on said substrate;
> an electrically conductive second plate (100B) disposed vertically above said first plate;
> an electrically conductive layer (100A) disposed between said first and second plates;
> at least one nanotube having an end electrically coupled with said first plate for increasing an effective area of said first plate, said at least one nanotube positioned in said electrically conductive layer; and
> a dielectric layer (101A) coating said length of said at least one nanotube such that said at least one nanotube is electrically isolated from said electrically-conductive layer and said second plate[.]

In contrast to the Examiner's contention, *Jin* fails to disclose or suggest "said at least one nanotube positioned in said electrically-conductive layer." Appellants submit that a person having ordinary skill in the art would understand that the nanotubes (103) in *Jin* are not positioned "in" the electrically-conducting layer (100A) disposed between the electrically-conducting plates (100B, 104).

According to MPEP § 2111.01, words of the claim must be given their plain (i.e., ordinary and customary) meaning unless a clear definition is provided in the specification. The plain meaning is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application. Appellants agree with the Examiner's statement on page 3 of the August 3, 2006 Office Action that the plain meaning of the term "in" would have been "to indicate inclusion, location or position within limits." *See, e.g.,* The American Heritage Dictionary, 3rd Ed., p. 684.

The electrically-conductive layer (100A) in *Jin* has a planar top surface and a planar bottom surface separated from the planar top surface by the layer thickness. The planar bottom

surface of the electrically-conductive layer (100A) is positioned closest to the first electrically-conductive plate (104). *Jin* discloses that the nanotubes (103) are placed on electrically-conductive layer 104 before layers (100A, 100B, 101A) are formed. *See Jin* at column 14, lines 28-35. Particles (107), which are removed from the final structure, mask regions of the nanotubes (103) during the formation of the layers of a grid structure, which includes layers (100A, 100B, 101A). *Id.*

A person having ordinary skill in the art would appreciate that the height of the nanotubes (103) that are visible in Figure 11 of *Jin* is representative of the height of the nanotubes (103) at any location on the substrate (105). This includes the locations on the substrate (105) covered by the grid structure and, specifically, the locations on the substrate (105) covered by the layers (101A, 100A, 100B) of the grid structure. Consequently and as apparent from Figure 11 of *Jin*, the nanotubes (103) coated by the dielectric layer (101A) fail to extend to even the bottom surface of the electrically-conductive layer (100A), much less to a position between the top and bottom surfaces of the electrically-conductive layer (100A). Based upon the plain meaning of the term "in" reproduced hereinabove, a person having ordinary skill in the art would understand that the pertinent "limits" of the electrically-conductive layer (100A) are the planar top and bottom surfaces. A person having ordinary skill in the art would further understand that no portion of any of the nanotubes (103) is included, located, or positioned, as required by the plain meaning of the term "in", between the planar top and bottom surfaces (i.e., the limits) of the electrically-conductive layer (100A). Instead, the bottom surface of the electrically-conductive layer (100A) is separated from the nearest portion of the nanotubes (103) by the majority of the thickness of the dielectric layer (101A). Hence, given the plain meaning of the term "in", a person having ordinary skill in the art would recognize that the nanotubes (103) are not "in" the electrically-conductive layer (100A).

If a reference fails to teach even one of the claimed elements, the reference does not and cannot anticipate the claimed invention. Because *Jin* fails to disclose "said at least one nanotube positioned in said electrically-conductive layer" as set forth in Appellants' independent claim 25, reversal of the Examiner's rejection of claim 1 under 35 U.S.C. § 102(b) is therefore respectfully requested for this reason alone.

Dependent Claims 26-28

Claims 26-28, which depend either directly or indirectly from independent claim 25, are not argued separately.

B. *Claims 1, 4-6, 8, and 10 were improperly rejected under 35 U.S.C. § 102(e) as being anticipated by Farnworth.*

The Examiner argues that *Farnworth* anticipates claims 1, 4-6, 8, and 10. As remarked above, anticipation of a claim under 35 U.S.C. § 102, however, requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros., Inc. v. Union Oil Co., 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), *quoted in* In re Robertson, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999). Absent express description, anticipation under inherency requires extrinsic evidence that makes it clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991), *quoted in* In re Robertson at 1951. "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Continental Can at 1749, *quoted in* In re Robertson at 1951.

Appellants respectfully submit that *Farnworth* fails to anticipate claims 1, 4-6, 8, and 10 and, as such, the rejections thereof should be reversed. Appellants will hereinafter address the various claims that are the subject of the Examiner's rejection in order.

Independent Claim 1

On pages 3 and 4 of the August 3, 2006 Office Action, the Examiner refers to Figure 1 of *Farnworth* and reproduces Appellants' independent claim 1 to contend that *Farnworth* discloses (indented for clarity):

> a substrate (12) defining a substantially horizontal plane;
> a source region (17);
> a drain region (21);
> a gate electrode (19) disposed on said substrate and being electrically insulated therefrom, said gate electrode positioned vertically between said source region and said drain region; and

> at least one semiconducting nanotube (22) including a first end electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source region and said drain region, said channel region being electrically insulated from said gate electrode, and
>
> said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of said at least one semiconducting nanotube between said source region and said drain region (column 3, lines 55-56 and column 7, lines 41-42).

In contrast to the Examiner's contention, a person having ordinary skill in the art would understand that *Farnworth* fails to disclose or suggest a nanotube that includes "a first end electrically coupled with said source region" and "a second end electrically coupled with said drain region." According to MPEP § 2111.01, words of the claim must be given their plain (i.e., ordinary and customary) meaning unless a clear definition is provided in the specification. The plain meaning is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application. The plain meaning of the term "end" would have been "either extremity of something that has a length." *See, e.g.,* The American Heritage Dictionary, 3rd Ed., p. 453. "Extremity" may be defined as "the outermost or farthest point or portion." *See, e.g.,* The American Heritage Dictionary, 3rd Ed., p. 486. The nanotube (22) in *Farnworth* has an inverted U-shape. Based on the plain meaning of the term "end" and the definition of "extremity," a person having ordinary skill in the art would comprehend that a first "end" of the U-shaped nanotube (22) in *Farnworth* is electrically coupled with the source (17) of device (10). However, the second "end" of the U-shaped nanotube (22) is <u>not</u> electrically coupled with the drain (21) of device (10). Instead, the first and second ends (i.e., the lengthwise extremities) of the nanotube (22) are electrically coupled with the source (17).

If a reference fails to teach even one of the claimed elements, the reference does not and cannot anticipate the claimed invention. Because *Farnworth* fails to disclose that the nanotube includes "a first end electrically coupled with said source region" and "a second end electrically coupled with said drain region" as set forth in Appellants' independent claim 25, reversal of the

Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(b) is therefore respectfully requested for this reason alone.

The Examiner states on page 7 of the August 3, 2006 Office Action that:

> A transistor operates by movement of electrons in the channel region inbetween the source and drain regions. Therefore, two outermost portions of the channel region/nanotube are electrically coupled with the source region and the drain region. Note that a channel region/nanotube is a three dimensional element, and each outermost portion of said element can be considered as an "end."

By way of rebuttal and as the Examiner's statement is best understood by Appellants' representative, Appellants believe that the Examiner errs in his construction of the device (10) disclosed in *Farnworth*. Specifically, the Examiner erroneously considers the entire length of the nanotube in *Farnworth* to be a channel region. When gated, current flows between the source (17) and drain (21) of device (10). *See* column 3, lines 53-66. Current does not flow in the portion of the U-shaped electrode above the drain (21) in Figure 1. Based upon this disclosure in *Farnworth*, a person having ordinary skill in the art would understand that the channel region of the transistor consists of the portion of the U-shaped nanotube (22) between the source (17) and the drain (21).

Appellants agree with the Examiner's statement that the nanotube (22) is a three dimensional element. Specifically and as remarked above, the nanotube (22) in *Farnworth* has a U-shape. Appellants agree with the Examiner's statement that the channel region is a three dimensional element. Specifically, the channel region of the device (10) in *Farnworth* consists of the two lengths of the nanotube (22) between the source (17) and drain (21). However, the channel region of the device (10) represents only a portion of the entire U-shaped nanotube (22). Consequently and given the plain meaning of the term "end", the nanotube (22) does not have an "end" electrically coupled with the drain (21).

Similarly, *Farnworth* discloses a device (70) in relation to Figure 5 that includes a nanotube (22), a source (77), and a drain (83). The nanotube (22) is linear. As indicated by the Examiner in the statement reproduced above, *Farnworth* discloses that current flows through the nanotube (22) between the source (77) and drain (83) to define a channel region between the source (77) and drain (83). However, current does not flow through the length of the nanotube

(22) above the drain (83). Consequently and given the plain meaning of the term "end", the nanotube (22) does not have an "end" electrically coupled with the drain (83).

For these additional reasons, *Farnworth* fails to disclose that the nanotube includes "a first end electrically coupled with said source region" and "a second end electrically coupled with said drain region" as set forth in Appellants' independent claim 25. Accordingly, reversal of the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(b) is therefore respectfully requested.

Dependent Claims 4-6, 8, and 10

Claims 4-6, 8, and 10, which depend either directly or indirectly from independent claim 1, are not argued separately.

C. *Claims 2, 3, and 9 were improperly rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnworth.*

Claims 2, 3, and 9, which depend from independent claim 1, are not argued separately.

VIII. Conclusion

In conclusion, Appellants respectfully request that the Board reverse the Examiner's rejections of claims 1-6, 8-10, and 25-28, and that the application be passed to issue. If there are any questions regarding the foregoing, please contact the undersigned. Moreover, if any other charges or credits are necessary to complete this communication, please apply them to Deposit Account 23-3000.

Respectfully submitted,
WOOD, HERRON & EVANS, L.L.P.

Date: October 27, 2006

By: /William R. Allen/
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APPENDIX OF CLAIMS

1. (Previously Presented) A semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a source region;

a drain region;

a gate electrode disposed on said substrate and being electrically insulated therefrom, said gate electrode positioned vertically between said source region and said drain region; and

at least one semiconducting nanotube including a first end electrically coupled with said source region, a second end electrically coupled with said drain region, and a channel region extending vertically through said gate electrode between said source region and said drain region, said channel region being electrically insulated from said gate electrode, and said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of said at least one semiconducting nanotube between said source region and said drain region.

2. (Original) The semiconductor device structure of claim 1 wherein said source is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

3. (Previously Presented) The semiconductor device structure of claim 1 wherein said drain is composed of a catalyst material effective for growing said at least one semiconducting nanotube.

4. (Original) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said drain and said gate electrode for electrically isolating said drain from said gate electrode.

5. (Original) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said source and said gate electrode for electrically isolating said source from said gate electrode.

6. (Previously Presented) The semiconductor device structure of claim 1 wherein said at least one semiconducting nanotube is composed of arranged carbon atoms.

7. (Cancelled)

8. (Previously Presented) The semiconductor device structure of claim 1 wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

9. (Previously Presented) The semiconductor device structure of claim 1 further comprising:
a plurality of semiconducting nanotubes extending vertically through said gate electrode.

10. (Previously Presented) The semiconductor device structure of claim 1 wherein said gate dielectric is disposed on said at least one semiconducting nanotube.

11-24. (Cancelled)

25. (Previously Presented) A semiconductor device structure, comprising:

a substrate;

an electrically-conductive first plate on said substrate;

an electrically-conductive second plate disposed vertically above said first plate;

an electrically-conductive layer disposed between said first and second plates;

at least one nanotube having an end electrically coupled with said first plate for increasing an effective area of said first plate, said at least one nanotube positioned in said electrically-conductive layer; and

a dielectric layer coating said length of said at least one nanotube such that said at least one nanotube is electrically isolated from said electrically-conductive layer and said second plate.

26. (Original) The semiconductor device structure of claim 25 wherein said at least one nanotube has a conducting molecular structure.

27. (Original) The semiconductor device structure of claim 25 wherein said at least one nanotube has a semiconducting molecular structure.

28. (Original) The semiconductor device structure of claim 25 wherein said dielectric layer encases said at least one nanotube.

29-33. (Cancelled)

APPENDIX OF EVIDENCE

(None)

APPENDIX OF RELATED PROCEEDINGS

(None)